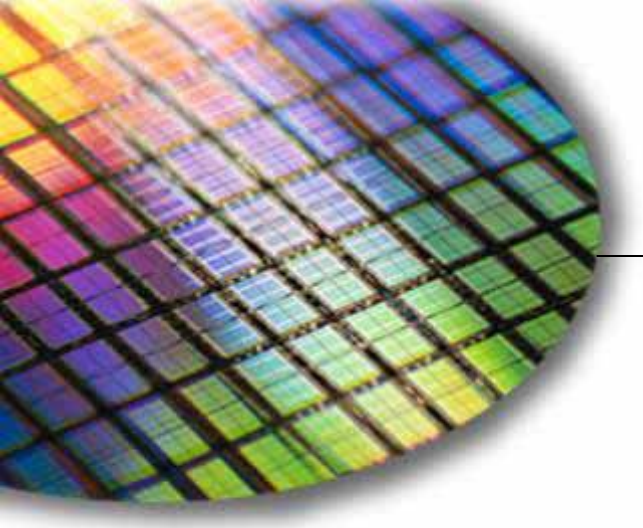


The World Leader in High Performance Signal Processing Solutions

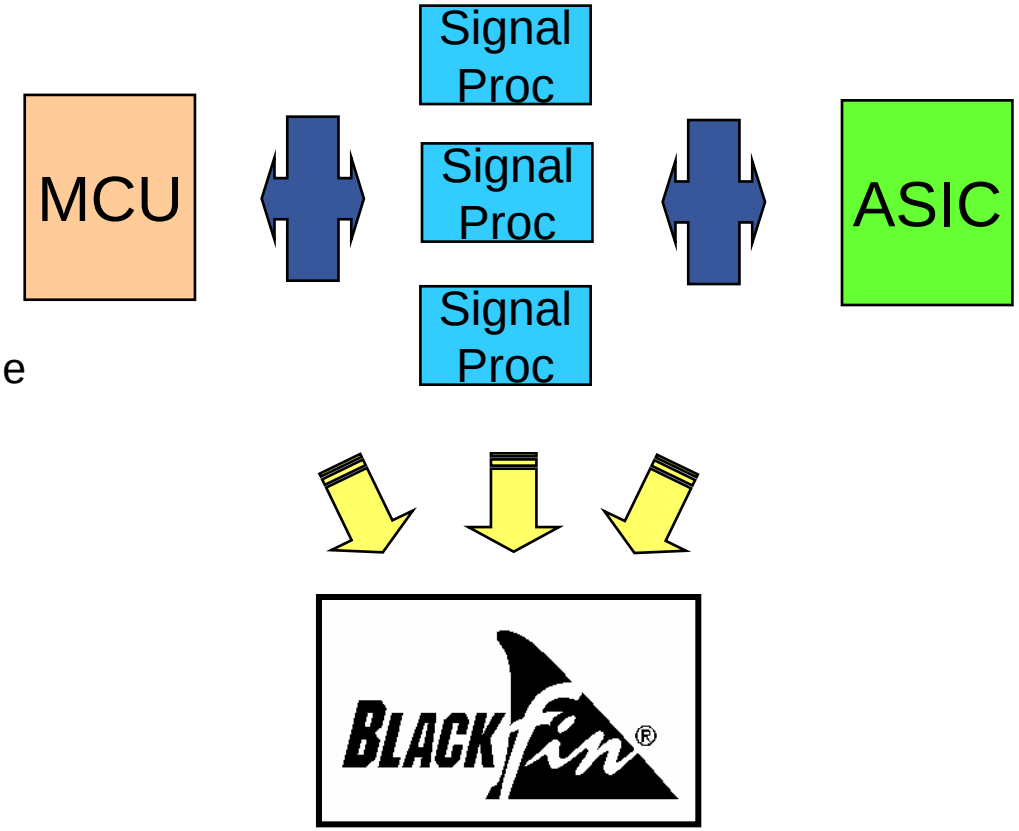
BLACKfin®

BF54x & BF52x Specifics & Status

ANALOG DEVICES

Blackfin Processors
Signal Processing and Micro-controller Functions

Control
Networking
RTC
Watchdog
RTOS
(MMU)
Byte addressable



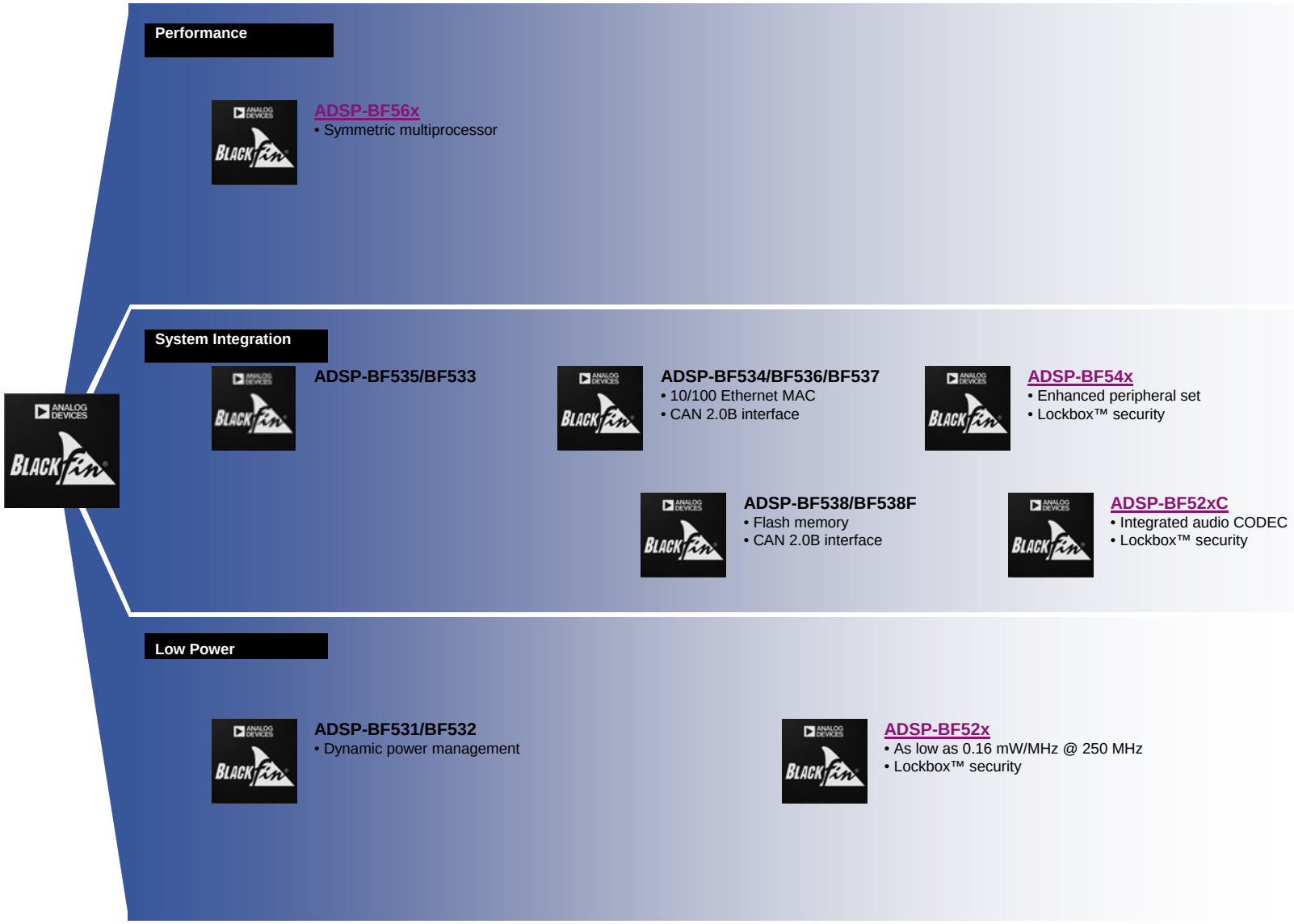
Interfaces to sensors
Broad peripheral mix
Memory

Blackfin can perform all of these functions!

Blackfin Architecture

- **The Blackfin architecture was crafted with the requirements of a controller and a DSP in mind**
  - **16/32-bit RISC MCU instruction set, 16-bit fixed-point dual MAC and four 8-bit ALUs**
  - **Ethernet, CAN, GPIO, SPI, USB, UART, TWI, RTC, SPORT, Timers, Watchdog**
  - **Storage options: NAND Flash, SDIO, ATAPI**
  - **Optimized to perform EQUALLY well on both control and/or numeric algorithms**
  - **Dynamic Power Management**
  - **Glueless interface to many converter devices or LCDs through (Enhanced) Parallel Peripheral Interface**

Blackfin Processor Product Portfolio



Blackfin ADSP-BF52x Family Portfolio

System Integration

- 533/600 MHz
- 132 KB RAM
- Integrated peripherals
- Lockbox™ security
- Stereo audio CODEC
- $13.46–$22.28

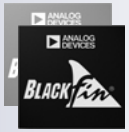
BF527/BF527C
- HS USB OTG
- 10/100 Ethernet
- HDMA

BF525/BF525C
- HS USB OTG
- HDMA

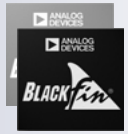
BF523/BF523C
- HDMA

Portable–Low Power

- 300/400 MHz
- 132 KB RAM
- 0.16 mW/MHz @ 250 MHz
- Lockbox™ security
- Stereo audio CODEC
- $7.78–$15.86



BF526/BF26C
- HS USB OTG
- 10/100 Ethernet
- HDMA



BF524/BF524C
- HS USB OTG
- HDMA

BF522/BF522C
- HDMA

Blackfin ADSP-BF54x Family Portfolio

System Integration

- Up to 600 MHz
- Up to 260 KB RAM
- DDR
- High bandwidth peripherals
- Lockbox™ security
- $13.98–$18.66

BF548/BF549C
- 260 KB RAM
- HS USB OTG
- ATAPI, SDIO, LCD
- Host DMA
- CAN 2.0B

BF544
- 196 KB RAM
- LCD, Tri-EPPI
- Host DMA

BF547
- 260 KB RAM
- HS USB OTG
- ATAPI, SDIO, LCD
- Host DMA

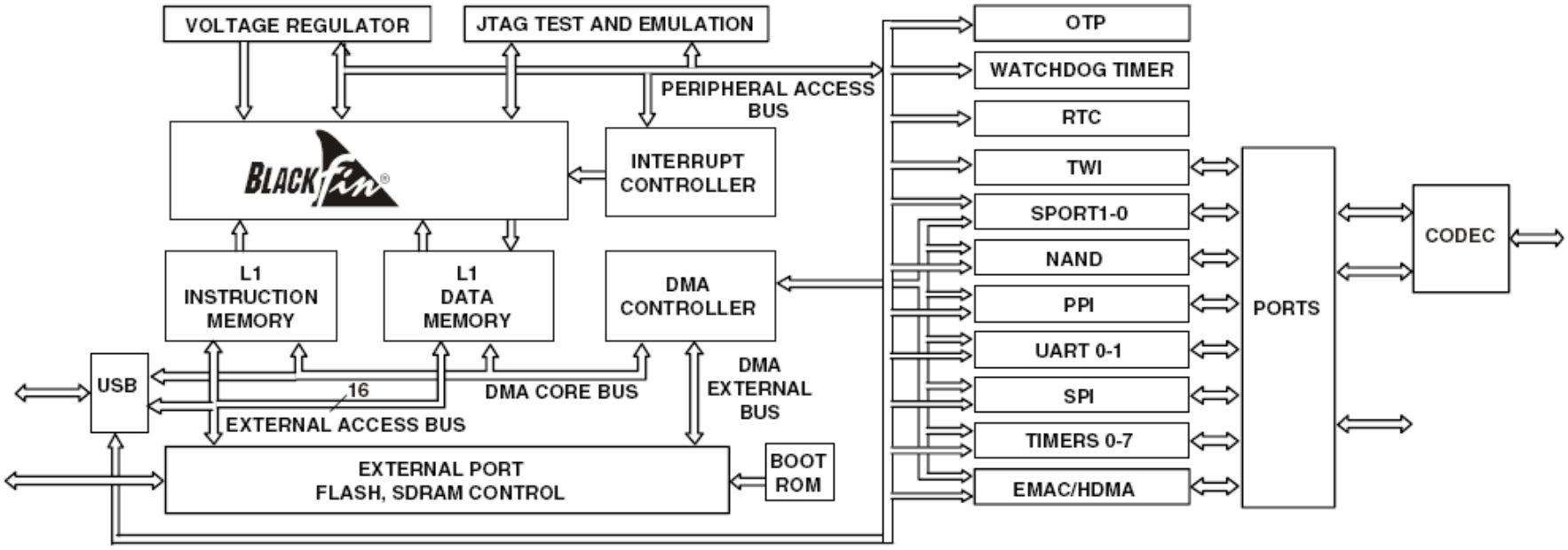
BF542
- 132 KB RAM
- HS USB OTG
- Dual EPPI

ADSP-BF52x Processors

- Pin- and code-compatible derivatives
- On-chip USB and Ethernet controllers
- New Lockbox Secure Technology
- Lowest Power Blackfin Processors
- Available with/without Stereo Audio CODEC: ADSP-BF52xC

	ADSP - BF527*/6	ADSP - BF525*/4	ADSP - BF523*/2
Performance	300, 400, 533*, 600* MHz, 600, 800, 1066*, 1200* MMACs	300, 400, 533*, 600* MHz, 600, 800, 1066*, 1200* MMACs	300, 400, 533*, 600* MHz, 600, 800, 1066*, 1200* MMACs
On Chip RAM	132 KBytes	132 KBytes	132 KBytes
Package Options	CSP_BGA	CSP_BGA	CSP_BGA

ADSP-BF52x/C Processors Architecture



ADSP-BF52x Processors Comparison Table

Feature	ADSP-BF522	ADSP-BF524	ADSP-BF526	ADSP-BF523	ADSP-BF525	ADSP-BF527
Host DMA	1	1	1	1	1	1
USB	x	1	1	x	1	1
Ethernet MAC	x	x	1	x	x	1
TWI	1	1	1	1	1	1
SPORTs	2	2	2	2	2	2
UARTs	2	2	2	2	2	2
SPI	1	1	1	1	1	1
GP Timers	8	8	8	8	8	8
Watchdog Timers	1	1	1	1	1	1
RTC	1	1	1	1	1	1
Parallel Peripheral Interface	1	1	1	1	1	1
GPIOs	48	48	48	48	48	48
Memory (bytes) L1 Instruction SRAM	48K	48K	48K	48K	48K	48K
Memory (bytes) L1 Instruction SRAM/Cache	16K	16K	16K	16K	16K	16K
Memory (bytes) L1 Data SRAM	32K	32K	32K	32K	32K	32K
Memory (bytes) L1 Data SRAM/Cache	32K	32K	32K	32K	32K	32K
Memory (bytes) L1 Scratchpad	4K	4K	4K	4K	4K	4K
Memory (bytes) L3 Boot ROM	32K	32K	32K	32K	32K	32K
Maximum Speed Grade	400 MHz			600 MHz		
Maximum System Clock Speed	80 MHz			133 MHz		
Package Options	289-Ball CSP_BGA					
	208-Ball CSP_BGA					

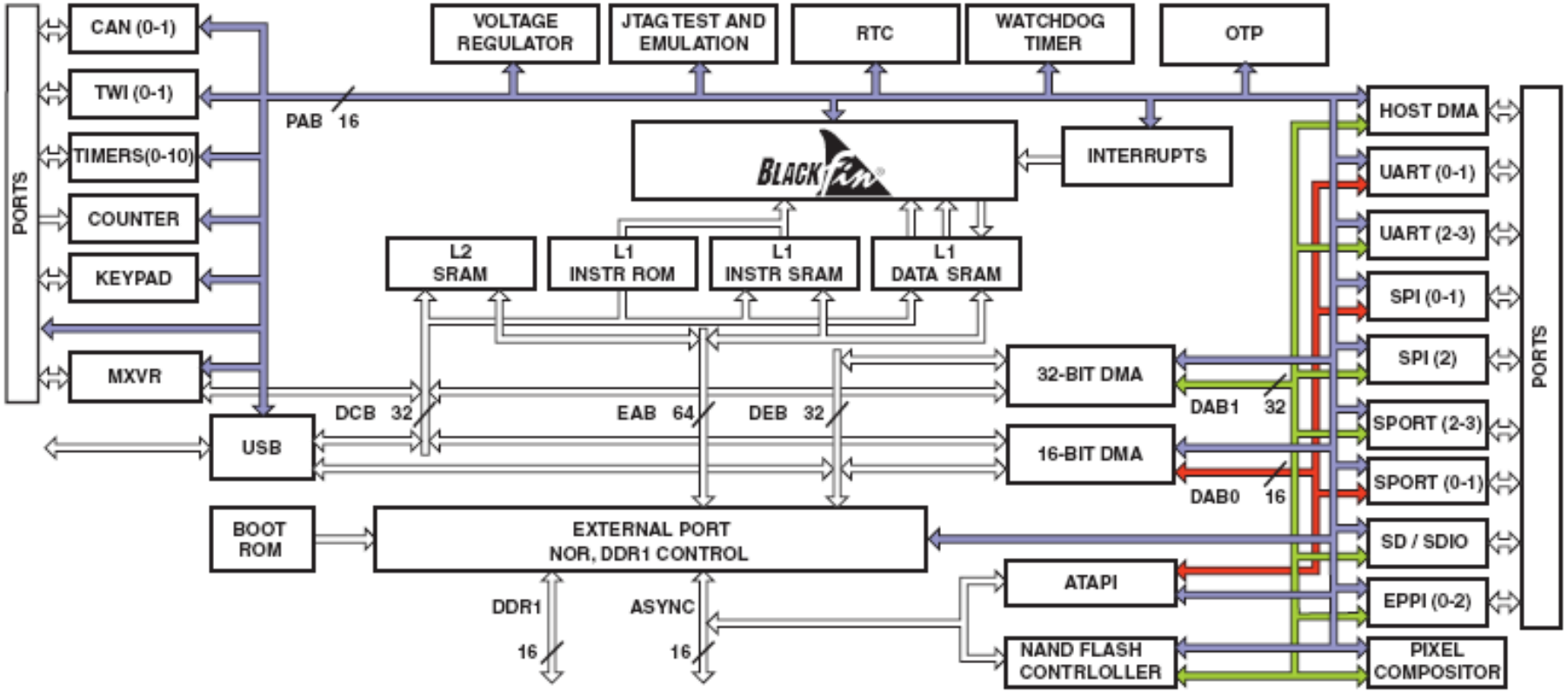
ADSP-BF549/8/7/4/2 Processors

- Pin- and code-compatible derivatives
- Enhanced peripheral set: EPPI, DDR, ATAPI, SD, NAND,…

	ADSP - BF549	ADSP - BF548	ADSP - BF547
Performance	533 MHz, 1066 MMACs	533, 600 MHz, 1066, 1200 MMACs	533, 600 MHz, 1066, 1200 MMACs
On Chip RAM	132 KBytes	132 KBytes	132 KBytes
Package Options	CSP_BGA	CSP_BGA	CSP_BGA

	ADSP - BF544	ADSP - BF542
Performance	400, 533 MHz, 800, 1066 MMACs	400, 533, 600 MHz, 800, 1066, 1200 MMACs
On Chip RAM	132 KBytes	132 KBytes
Package Options	CSP_BGA	CSP_BGA

ADSP-BF54x Processors Architecture



ADSP-BF54x Processors Comparison Table

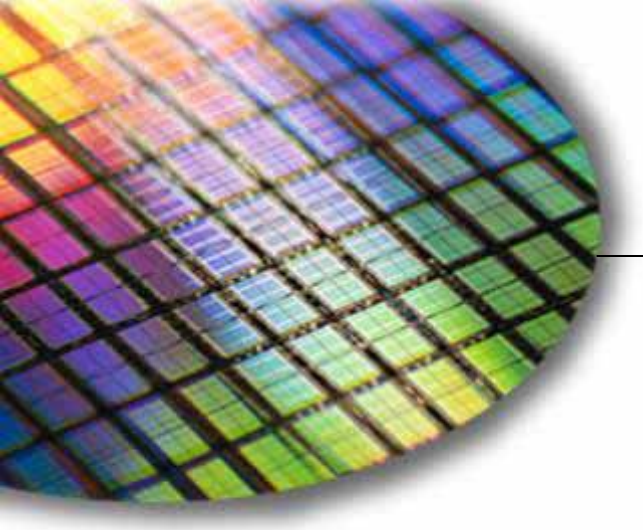
Table 1. ADSP-BF542/4/7/8/9 Processor Features

Processor Features		ADSP-BF549	ADSP-BF548	ADSP-BF547	ADSP-BF544	ADSP-BF542
Lockbox™ Code Security		1	1	1	1	1
SD/SDIO Controller		1	1	1	–	1
Pixel Compositor		1	1	1	1	1
18- or 24-bit EPPI0 with LCD		1	1	1	1	–
16-bit EPPI1, 8-bit EPPI2		1	1	1	1	1
Host DMA Port		1	1	1	1	–
NAND Flash Controller		1	1	1	1	1
ATAPI		1	1	1	–	1
High Speed USB OTG		1	1	1	–	1
Keypad Interface		1	1	1	–	1
MXVR		1	–	–	–	–
CAN ports[1]		2	2	–	2	1
TWI ports		2	2	2	2	1
SPI ports		3	3	3	2	2
UART ports		4	4	4	3	3
SPORTs		4	4	4	3	3
Up / Down Counter		1	1	1	1	1
Timers		11	11	11	11	8
General-purpose I/O pins		152	152	152	152	152
Memory Configurations (K Bytes)	L1 Instruction SRAM/Cache	16	16	16	16	16
	L1 Instruction SRAM	48	48	48	48	48
	L1 Data SRAM/Cache	32	32	32	32	32
	L1 Data SRAM	32	32	32	32	32
	L1 Scratchpad SRAM	4	4	4	4	4
	L1 ROM[2]	64	64	64	64	64
	L2	128	128	128	64	–
	L3 Boot ROM[2]	4	4	4	4	4
Maximum Core Instruction Rate (MHz)		533	600	600	533	600

[1] Automotive Only.
[2] This ROM is not customer configurable.

CROSSCORE Development Tools

- **Provides easier and more robust methods for engineers to develop and optimize systems**
- **Shortens product development cycles for faster time-to-market**
- **CROSSCORE includes:**
  - **VisualDSP++**
  - **Emulators**
    - USB
  - **Evaluation Boards**
    - EZ-KIT Lite (expandable)
  - **Single Board Computers**
    - Available for vertical applications:
      - digital media players
      - digital still and video cameras
      - automotive telematics
      - professional audio
      - videophones
      - and more
  - **Low Cost of Customer Ownership**
    - Free technical support
      - Integrated into VisualDSP++ environment
      - Equal attention to the smallest and largest of customers
    - No per-unit royalties or other per-unit costs
    - Free VisualDSP++ update and migration to future releases

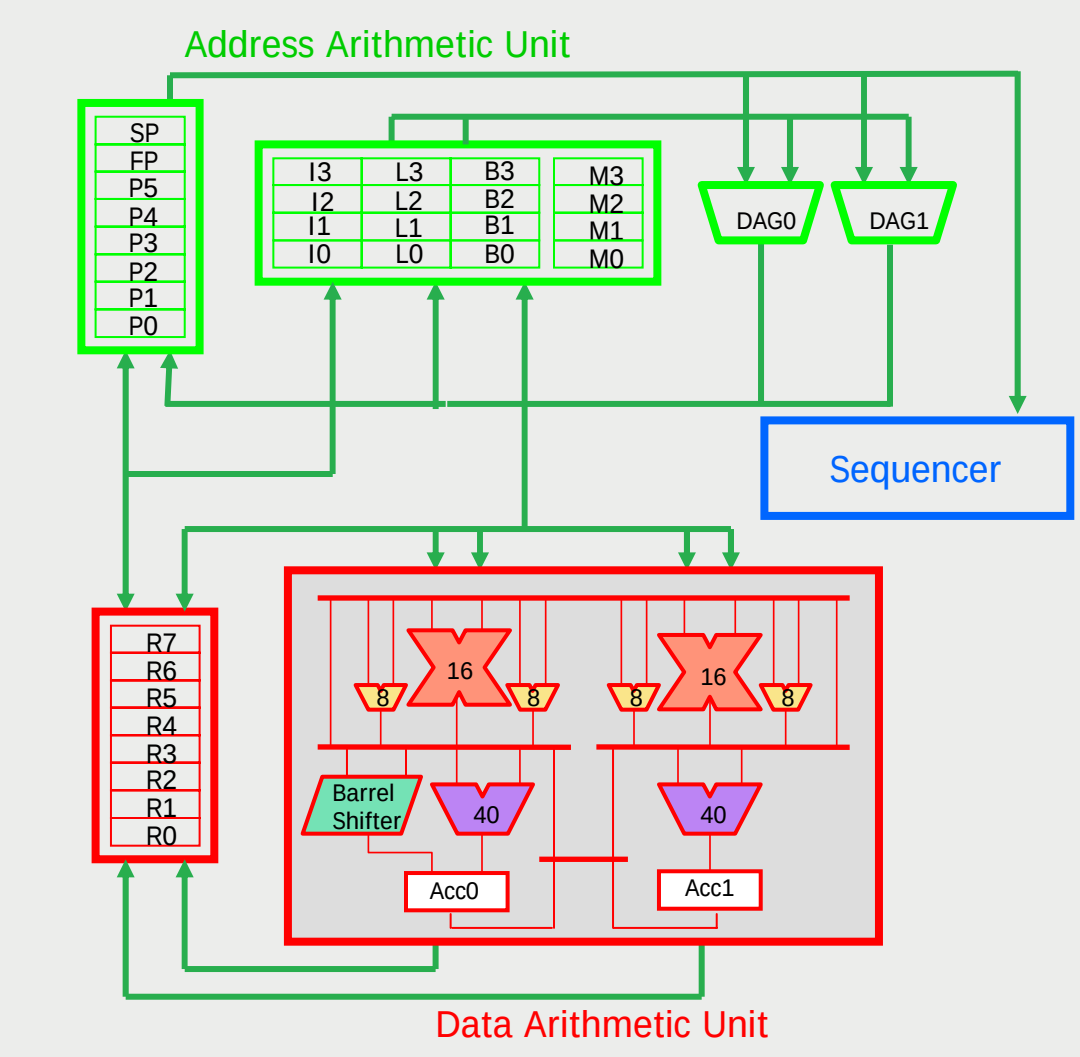


The World Leader in High Performance Signal Processing Solutions

Blackfin® Architecture

ANALOG DEVICES

Computational Units - Codecompatible



Two 32/40-bit ALUs

Two 16-bit Multipliers

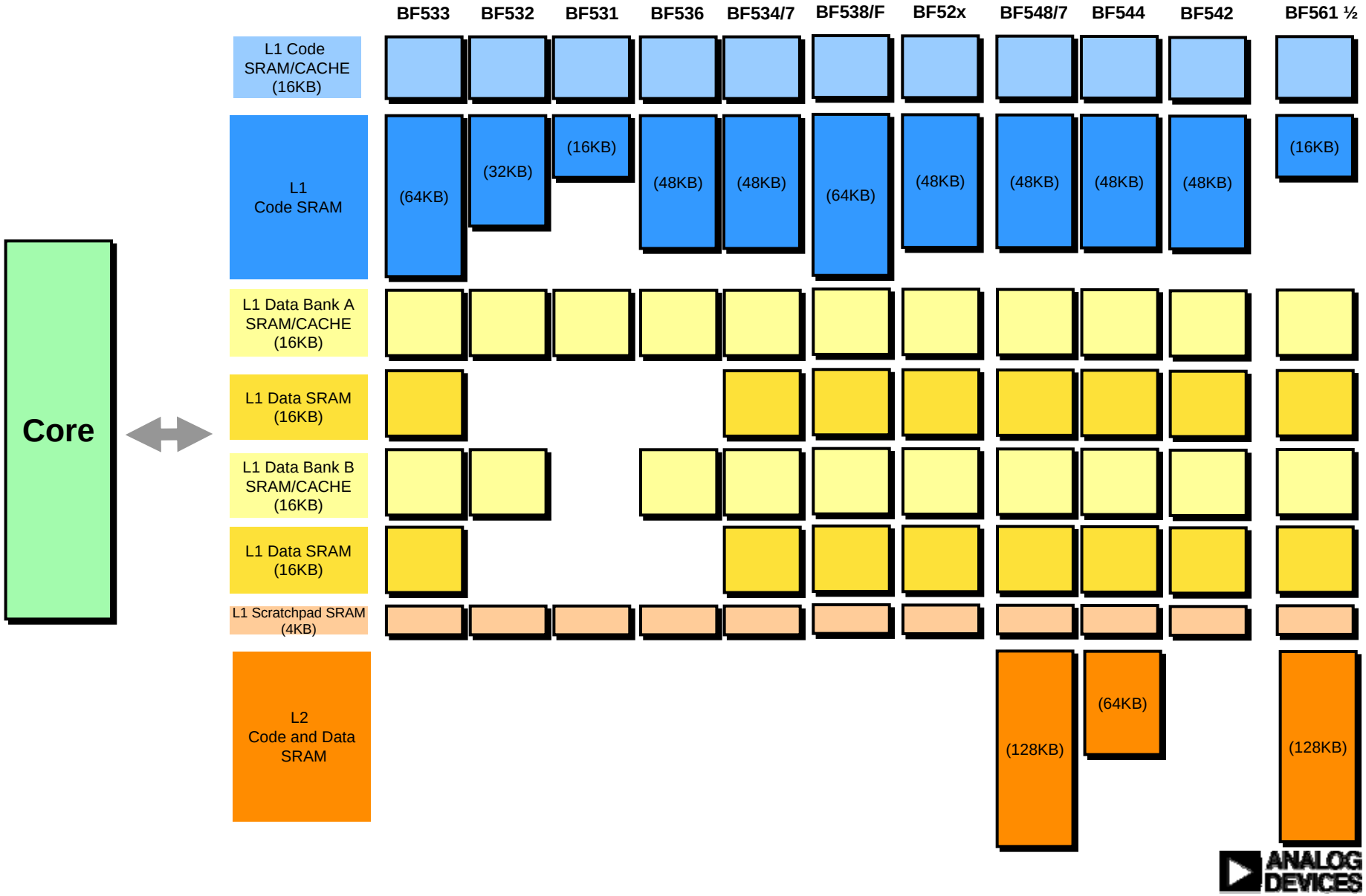
Four 8-bit Video ALUs

Barrel Shifter

Blackfin Memory

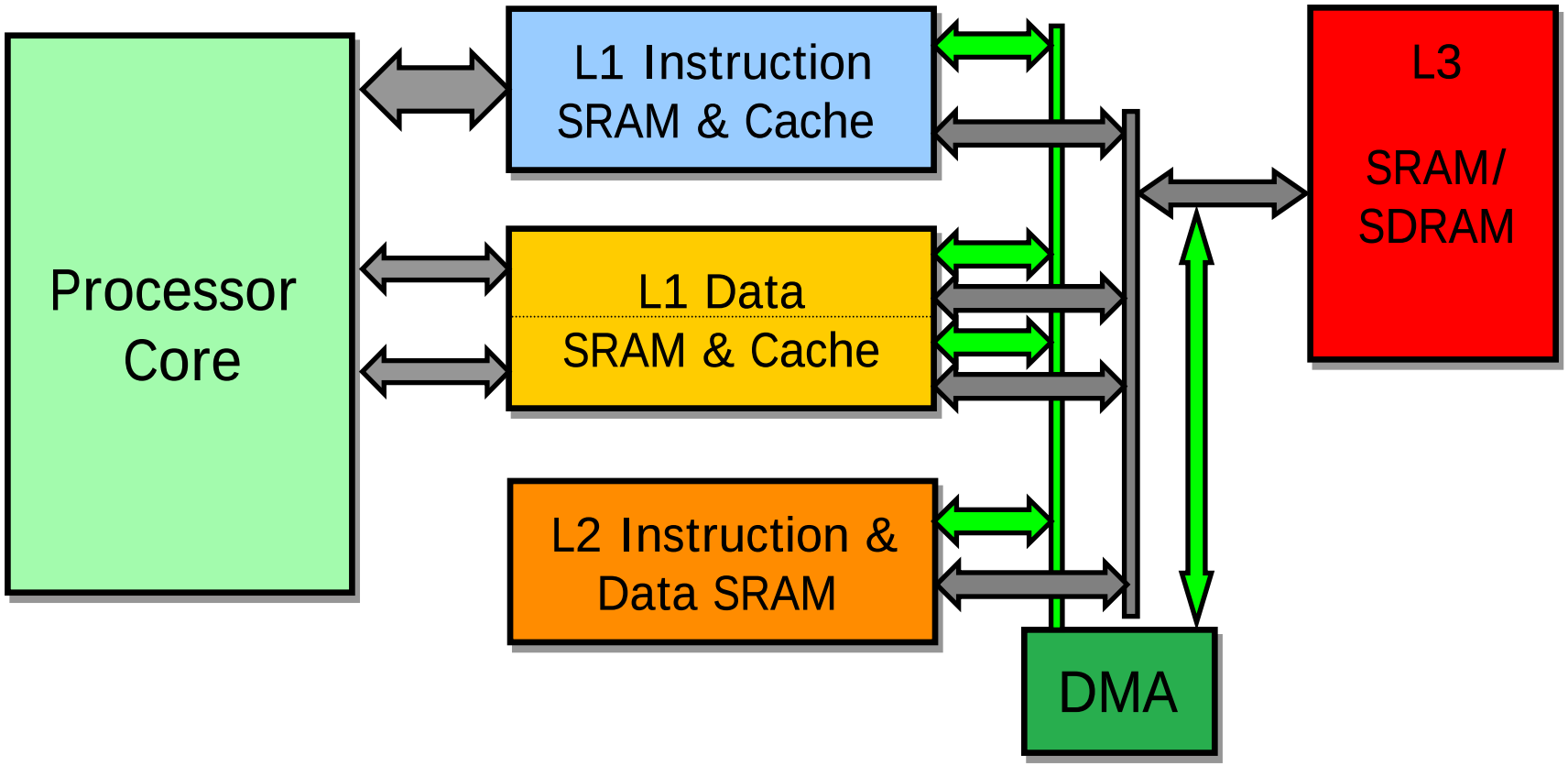
- **As processor speeds increase, it becomes increasingly difficult to have large memories running at full core speed**
- **Blackfin Processors use a memory hierarchy with a primary goal of achieving memory performance similar to that of the fastest memory (i.e. L1) with an overall cost close to that of the least expensive memory (i.e. L3)**
  - **L1 Memory**
    - Internal memory
    - Smallest density
    - Best performance
    - Operates at Core Clock (CCLK)
  - **L2 Memory**
    - Internal memory
    - Higher density
    - Slower performance
    - Operates at Half Core Clock (CCLK/2)
  - **L3 Memory**
    - External memory
    - Highest density
    - Slowest performance
    - Operates at System Clock (SCLK)

Blackfin Internal Memory



Memory System

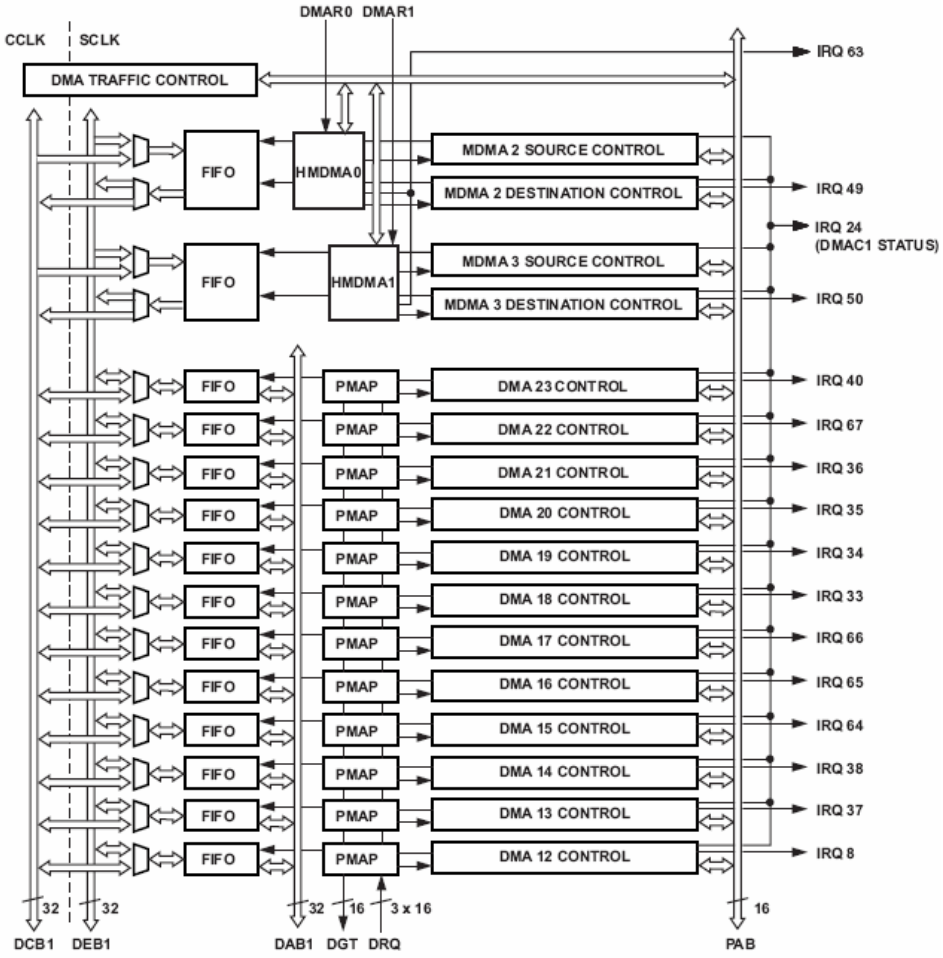
- **Separate Multi-ported Instruction and Data Memories**

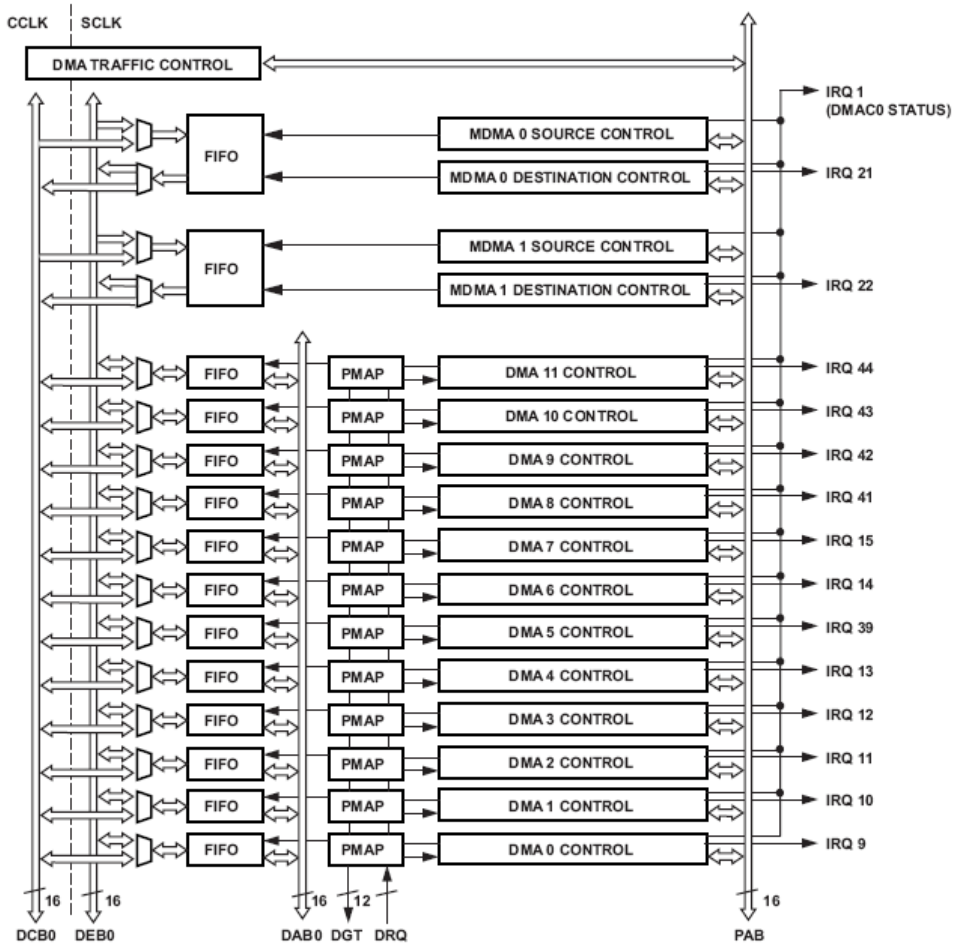


Direct Memory Access (DMA)

- **The Blackfin DMA controller allows data transfer operations without processor core intervention!**
- **Up to two DMA controllers**
  - **DMAC0 has a 16-bit data bus**
  - **DMAC1 has a 32-bit data bus**
- **The DMA controllers can perform several types of data transfers:**
  - **Peripheral DMA transfers data between memory and on-chip peripherals**
    - Serial Ports (SPORTx)
    - UARTx
    - PPI/EPPIx and HOST
    - Pixel Compositor (PIXC)
    - NAND Flash Controller (NFC) and Secure Digital Host (SDH)
    - ATAPI
    - SPIx
  - **Memory DMA (MDMA) transfers data between memory and memory**
    - MDMA3:0
  - **Handshaking Memory DMA (HMDMA) transfers data between off-chip peripherals and memory**
    - DMAR0 and DMAR1

DMA Controller Overview





Default Peripheral DMA Mapping

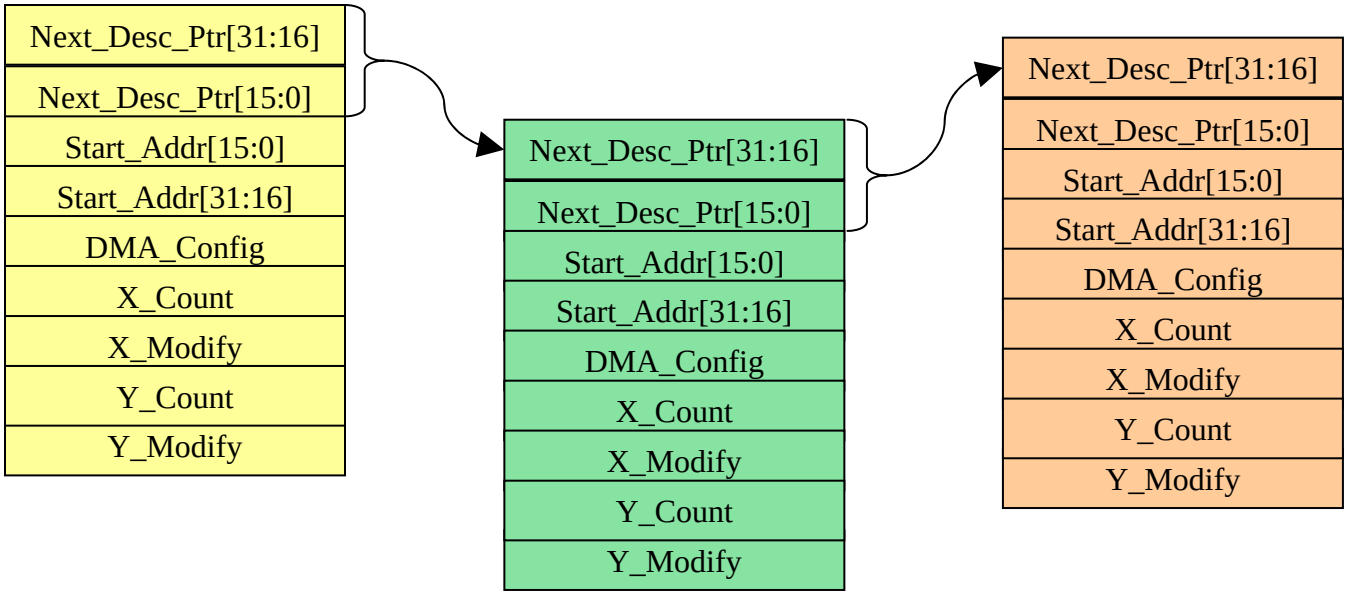
- The peripheral DMA channels in each controller work completely independently from each other
- The transfer timing is controlled by the mapped peripheral
- Users can change the priorities of DMAC0 and DMAC1
  - By default, DMA0 has higher priority than DMA1, and so on…and DMA11 has the lowest priority

DMA Channel	DMA Controller	PMAP Default[1, 2]	Peripheral Mapped by Default
DMA0	DMAC0	0x0	SPORT0 receive
DMA1	DMAC0	0x1	SPORT0 transmit
DMA2	DMAC0	0x2	SPORT1 receive
DMA3	DMAC0	0x3	SPORT1 transmit
DMA4	DMAC0	0x4	SPI0 receive/transmit
DMA5	DMAC0	0x5	SPI1 receive/transmit
DMA6	DMAC0	0x6	UART0 receive
DMA7	DMAC0	0x7	UART0 transmit
DMA8	DMAC0	0x8	UART1 receive
DMA9	DMAC0	0x9	UART1 transmit
DMA10	DMAC0	0xA	ATAPI receive
DMA11	DMAC0	0xB	ATAPI transmit
DMA12	DMAC1	0x0	EPPI0 receive/transmit
DMA13	DMAC1	0x1	EPPI1 receive/transmit
DMA14	DMAC1	0x2	EPPI2/Host DMA receive/transmit
DMA15	DMAC1	0x3	PIXC image data (read from memory)
DMA16	DMAC1	0x4	PIXC overlay data (read from memory)
DMA17	DMAC1	0x5	PIXC output data (write to memory)
DMA18	DMAC1	0x6	SPORT2 receive
DMA19	DMAC1	0x7	SPORT2 transmit
DMA20	DMAC1	0x8	SPORT3 receive
DMA21	DMAC1	0x9	SPORT3 transmit
DMA22	DMAC1	0xA	SDH/NFC receive/transmit
DMA23	DMAC1	0xB	SPI2 receive/transmit
–	DMAC1	0xC	Note[3]
–	DMAC1	0xD	Note[3]
–	DMAC1	0xE	Note[3]
–	DMAC1	0xF	Note[3]

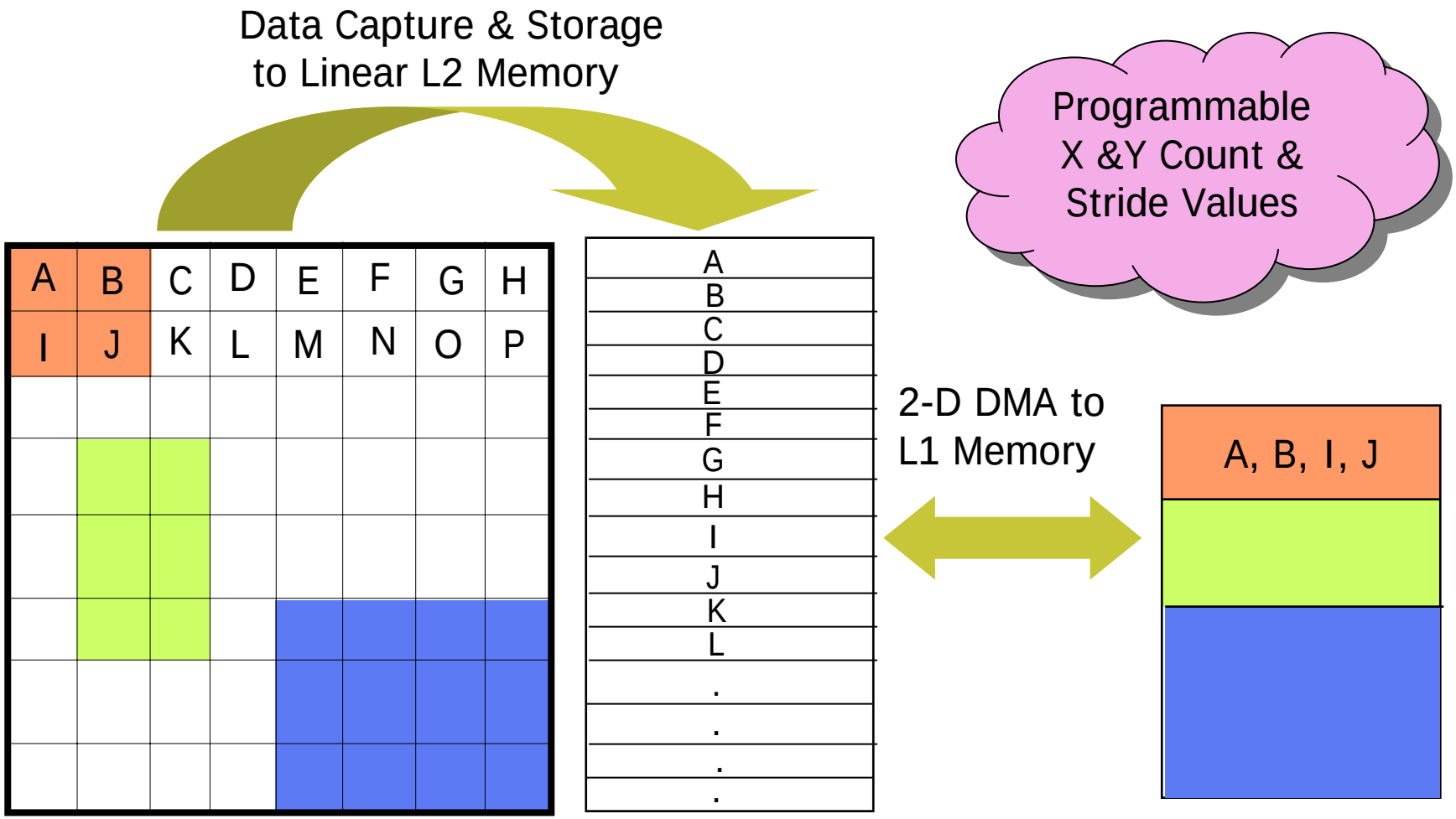
DMA Setup

- **Two Types of DMA transfers available**
- **Register-based**
  - **Program the DMA control registers directly**
  - **Upon DMA completion, control registers are automatically updated with their original setup values in Autobuffer Mode (multiple transfers)**
  - **The DMA Channel can also be configured to gracefully shut off with Stop Mode (single transfer)**
- **Descriptor-based**
  - **Requires a set of parameters stored within memory to initiate a DMA sequence.**
  - **Supports chaining of multiple DMA transfers**

Descriptor Blocks Example



2-D Direct Memory Access



2-D DMA significantly decreases S/W overhead in video applications!

Blackfin Peripherals

Peripheral	ADSP-BF531/BF532/BF533	ADSP-BF534	ADSP-BF536/BF537	ADSP-BF538/BF538F	ADSP-BF522/BF523	ADSP-BF524/BF525	ADSP-BF526/BF527	ADSP-BF542	ADSP-BF544	ADSP-BF547	ADSP-BF548	ADSP-BF561
SPI	1	1	1	3	1	1	1	2	2	3	3	1
SPORT	2	2	2	4	2	2	2	3	3	4	4	2
UART	1	2	2	3	2	2	2	3	3	4	4	1
GP Timers	3	8	8	3	8	8	8	11	11	8	8	12
Watchdog	1	1	1	1	1	1	1	1	1	1	1	2
USB 2.0 HS OTG	N	N	N	N	N	Y	Y	Y	N	Y	Y	N
RTC	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N
PPI	1	1	1	1	1	1	1	N	N	N	N	2
ePPI	N	N	N	N	N	N	N	2	3	3	3	N
PIXC	N	N	N	N	N	N	N	Y	Y	Y	Y	N
TWI	N	1	1	2	1	1	1	2	2	1	1	N
CAN	N	1	1	1	N	N	N	1*	2*	N	2	N
10/100 EMAC	N	N	Y	N	N	N	Y	N	N	N	N	N
Handshake DMA	N	Y	Y	N	N	N	N	Y	Y	Y	Y	N
Host Port DMA	N	N	N	N	Y	Y	Y	N	Y	Y	Y	N
SDIO	N	N	N	N	N	N	N	Y	N	Y	Y	N
ATAPI	N	N	N	N	N	N	N	Y	N	Y	Y	N
NAND Flash	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	N
Keypad	N	N	N	N	N	N	N	Y	N	Y	Y	N
Rotary Counter	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	N
Lockbox/OTP	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	N
					* Automotive grade parts ONLY							

ANALOG DEVICES

USB 2.0 High-Speed On-the-Go (HS OTG)

- **The on-chip USB controller can operate in:**
  - **Traditional USB peripheral-only mode**
  - **Host mode presented in the On-The-Go (OTG) supplement to the USB 2.0 Specification**
- **In host mode, the USB module supports transfers at:**
  - **High-speed (480Mbps)**
  - **Full-speed (12Mbps)**
  - **Low-speed (1.5Mbps)**
- **In peripheral mode supports:**
  - **High-speed**
  - **Full-speed**
- **USB OTG Controller features include:**
  - **1 bidirectional control endpoint, 7 transmit and 7 receive unidirectional endpoints**
  - **8 DMA master channels**
  - **3 top-level maskable general purpose interrupts**
  - **1 asynchronous wakeup interrupt**
  - **VBUS control interrupts for external analog VBUS control**
  - **Session request protocol (SRP) and host negotiation protocol (HNP) capability**
  - **Soft connect/disconnect feature**
- **USB Drivers included with VisualDSP++**
  - **Mass Storage class (Peripheral & Host)**
    - Uses File System system service
  - **Bulk driver examples**

Parallel Peripheral Interface (PPI)

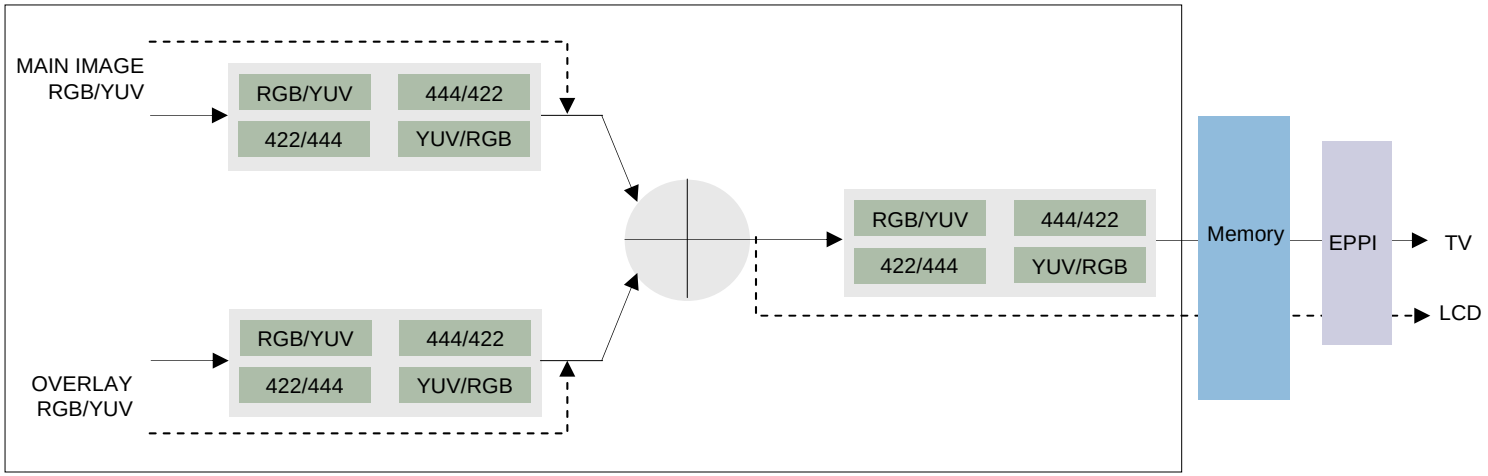
- **Programmable Data Length: 8, 10, 12, 14, or 16 bits per clock cycle**
- **Bidirectional (half-duplex) parallel interface**
- **Synchronous Interface**
  - **Interface is driven by an external clock (“PPI_CLK”)**
  - **Up to 66MHz rate (SCLK/2)**
  - **Asynchronous to SCLK**
- **Includes three frame syncs to control the interface timing**
- **Applications**
  - **Driving LCD Interface**
  - **General Purpose Interface to outside world**
  - **High speed data converters**
  - **Video CODECs**

Enhanced Parallel Peripheral Interface (EPPI)

- **Programmable Data Length: 8, 10, 12, 14, 16, 18 or 24 bits per clock cycle**
- **EPPI clock can be provided externally or internally**
  - **External clock: 75 MHz TX/RX @ 16 bits, allowing connection to popular ADI high-speed converters and HD video encoders/decoders**
  - **Internal clock: up to 66 MHz TX/RX, for SCLK=133 MHz**
- **ITU-R BT.656 Internal Blanking, Preamble and Status Word Generation for TX modes**
  - **Saves considerable DMA bandwidth by bypassing external memory**
- **Horizontal and Vertical Windowing of inbound/outbound data**
- **Programmable clipping of 8-bit output data**
- **Truncation of RGB888 values to RGB666 or RGB565 for flexible LCD connections**
  - **Allows easy connection to 24 bit (8-8-8), 18-bit (6-6-6) or 16-bit (5-6-5) LCDs**
- **De-interleaving/Interleaving Modes for 4:2:2 YCbCr data, allowing efficient DMA transfer in planar and interleaved buffer formats**
- **Optional sign-extension or zero-fill of received data**

Pixel Compositor (PIXC)

- **Why? Provides more MIPS for customer application**
- **What is it? Hardware acceleration to perform overlays, color conversion, and alpha blending**
  - **Significantly reduces processor core overhead associated with software RGB-YUV color conversion and alpha blending**
  - **Image/overlay from L1/L2/L3 memory**
  - **Provides image data stream for either active-matrix TFT LCD panel or analog NTSC/PAL DAC**
  - **Supports YUV 4:2:2 or RGB888 input/output data format**
  - **Overlay content transparency ratio control (alpha)**
  - **Support for transparent colors in the desired color space (RGB or YUV)**
  - **Programmable color space conversion on either the main image, the overlay image, or the blended output**



Two-Wire Interface (TWI)

- **Fully compliant to the Philips I2C bus protocol**
  - **See Philips I2C Bus Specification version 2.1**
    - 7-bit addressing
    - 100 Kb/s (normal mode) and 400Kb/s (fast mode) data rates
    - General call address support
- **Supports Master and Slave operation**
  - **Separate receive and transmit FIFOs**
- **SCCB (Serial Camera Control Bus) support**
  - **Only in Master mode**

Ethernet MAC Controller

- **Features:**
  - **MII/RMII interface**
  - **10Mbit/s and 100Mbit/s operation**
  - **VLAN support**
  - **Independent DMA-driven RX and TX channels**
  - **Automatic network monitoring statistics**
  - **Flexible address filtering and flexible event detection for interrupt**
  - **Validation of IP and TCP (payload) checksums**
  - **Remote-wakeup Ethernet frames**
  - **Network-aware system power management**
- **VisualDSP++ Ethernet Support:**
  - **LwIP stack (open source) ported to Blackfin**
    - Basic feature set (sockets, DHCP client)
  - **Supported hardware configurations are:**
    - ADSP-BF537 and ADSP-BF527 EZ-KIT Lite
    - With external MAC or EZ-USBLAN EZEXT daughter card, also:
      - ADSP-BF548 EZ-KIT Lite
      - ADSP-BF533 EZ-KIT Lite
      - ADSP-BF538 EZ-KIT Lite
      - ADSP-BF561 EZ-KIT Lite
  - **Supported OS configurations:**
    - VDK
  - **System Builder wizard to create a “ping-able” project out-of-the-box**
    - Create a skeleton project that receives an IP address via DHCP and then idles, listening for connections (which the user defines)
  - **Examples for DNS look-up, telnet hosts, more**

Host DMA Port

- **The Host DMA port (HOSTDP) facilitates a host device external to the Blackfin processor to be a DMA master and transfer data back and forth**
- **The host device always masters the transactions and the processor is always a DMA slave device**
- **The Host DMA Port controller includes the following features:**
  - **Allows an external master to configure DMA read/write data transfers and read port status**
  - **Uses a flexible asynchronous memory protocol for its external interface**
  - **Allows an 8- or 16-bit external data interface to the host device**
  - **Supports half-duplex operation**
  - **Supports little/big endian data transfers**
  - **Supports two modes of operation**
    - Acknowledge mode allows flow control on host transactions
    - Interrupt mode guarantees a burst of FIFO depth host transactions

ATAPI and Secure Digital Host (SDH)

- **ATAPI-6 Controller**
  - **Interfaces with hard drives and DVD/CD drives, as well as CompactFlash in TrueIDE mode**
  - **Separate interface from DDR memory subsystem for access to HDD, DVD, etc.**
  - **Supports max DVD transfer rates**
  - **Multiplexed with Asynchronous memory interface**
- **Secure Digital Host (SDH)**
  - **1 to 4-bit port for connection to SD memory cards and SDIO modules like WLAN and Bluetooth**
    - 'SPI mode' not supported
  - **Supports single MMC, SD or SDIO card at a time**
  - **Offers card detection via one of the data pins**
  - **Supports SDIO interrupt and read wait features**

NAND Flash Controller (NFC)

- Dedicated hardware support for interfacing to Single Level Cell (SLC) NAND flash memories
- Device access timing control for read and write strobes
- Direct support for 256-Byte and 512-Byte page sizes
- Dedicated hardware for generation of ECC parity data
- Support for all NAND flash commands
- Support for 8-bit /16-bit NAND Flash Interfaces
- Directly supports SLC NAND flash devices of unlimited size
- Can release external bus interface pins during long accesses for peripheral sharing
- DMA interface for efficient page program and page read operations

Up/Down Counter

- **Rotary (up/down) Counter provides support for manually controlled rotary controllers**
  - **Ex.: Volume wheel on a radio device**
- **The Rotary Counter includes the following features:**
  - **32-bit Up/Down Counter**
  - **Quadrature Encoder mode (Gray code)**
  - **Binary Encoder mode**
  - **Alternative Frequency-Direction mode**
  - **Timed Direction and Up/Down Counting modes**
  - **Zero Marker / Push Button support**
  - **Capture Event Timing in association with GP Timer**
  - **Boundary Comparison and Boundary Setting features**
  - **Input Pin Noise Filtering (de-bouncing)**
  - **Flexible Error Detection/Signaling**

Keypad

- **The keypad is a 16 pin Interface module that is used to detect the key pressed in an 8x8 (maximum) keypad matrix**
- **The keypad module supports two modes of operation:**
  - **Press-Release-Press mode**
    - Identifies a press-release-press sequence of a key as two consecutive presses of the same key
  - **Press-Hold mode**
    - Checks the input key's state in periodic intervals to determine the number of times the same key is meant to be pressed
- **Programmable input keypad matrix size**
- **Programmable debounce filter width**
- **Interrupt on any key pressed capability**
- **Multiple key pressed detection and limited multiple key resolution capability**

External Bus Interface Unit (EBIU)

- **Glueless interface to synchronous and asynchronous memories**
- **Asynchronous Memory Interface**
  - **Supports interfacing to memories such as SRAM and FLASH devices**
  - **Up to 256 MB supported across 4 memory banks**
  - **Supports page mode and burst mode reads**
- **Synchronous Memory Interface**
  - **DDR1 SDRAM interface (ADSP-BF54x only)**
    - 16-bit pin interface, leading to 32 bits of data on every SCLK cycle
    - Operates at max of 266 Mwords/sec (at SCLK=133 MHz)
    - Up to 512 MB supported on 2 external DDR memory banks
    - Separate supply from Async Memory Interface
      - DDR is supported at 2.5V DDR supply
      - Mobile DDR is supported at 1.8V DDR supply
  - **SDRAM interface (all except ADSP-BF54x)**

Lockbox™ Secure Technology for Blackfin

- **New Lockbox Secure Technology introduced with ADSP-BF54x/ADSP-BF52x Blackfin Processors**
- **Blackfin Lockbox technology is composed of a mix of hardware and software mechanisms**
- **Designed to prevent unauthorized access and allow only trusted code to execute on the processor**
- **Security Benefits**
  - **IP protection**
    - Ensure code has not been altered and comes from the appropriate source through authentication
    - Verify a code or data image against its embedded digital signature
  - **Prevention of mass copying**
    - Support cryptographic encryption/decryption when confidentiality is required
    - Utilize unique chip ID to “lock” processor to one specific boot source/device
  - **Digital rights management**
    - Identify valid media content

Blackfin Enhancements for Security
List of new hardware features

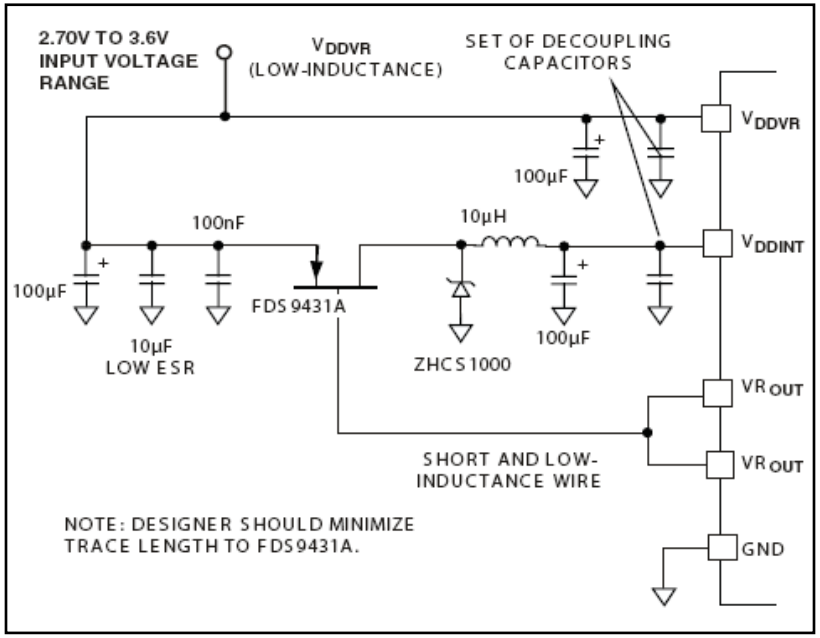
- **One Time Programmable memory**
  - **Public OTP memory (4 KBytes)**
    - Used to keep a trusted Public Key for proper authentication
  - **Private (secret) OTP memory (4 KBytes)**
    - Used to keep secrets only accessible in Secure Mode (example: secret keys for a cipher)
  - **Unique Chip ID (stored in Public OTP memory)**
    - Can be used to prevent cloning of products (bind software -in a flash memory- to a single Processor)
- **Secure ROM**
    - Used to store the authentication software (Secure Entry Service Routine, crypto)
- **Secure State Machine**
  - **Open Mode (Unsecured)**
    - Default power up mode of the Processor
  - **Secure Entry Mode**
    - Ensures integrity of authentication process
  - **Secure Mode**
    - Secure environment to execute sensitive code and protect data in on-chip memory
- **Hardware Monitor**
  - **Firmware execution is monitored for unexpected branches**
- **System switches (SECURE_SYSSWT)**
  - **Controls secure environment and prevents attacks using JTAG, reset pin or DMA memory accesses**

Dynamic Power Management

- **Blackfin Processors provide 5 operating modes:**
  - **Full-On**
    - This is the power-up default execution state in which maximum performance can be achieved
    - The processor core and all enabled peripherals run at full speed
  - **Active**
    - PLL is enabled but bypassed
    - Thus, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency
  - **Sleep**
    - Core is disabled but peripherals enabled
    - Peripheral Interrupts can wake up the Core
  - **Deep Sleep**
    - Core and Peripherals disabled
    - Wake up: Reset or RTC
  - **Hibernate**
    - Maximum Power Savings
    - Core power switched off
    - Wake up: Reset, RTC, CAN, Ethernet, Keypad, Up/Down Counter, USB and some GPIOs
    - Reboot always necessary

On-chip Voltage Regulation

- On-chip voltage regulator that generates core voltage levels from an external supply
- The regulator controls the internal voltage levels in increments of 50 mV (programmable)
- The regulator can be disabled and bypassed
- Minimum external components required
- See EE-228: Switching Regulator Design Considerations for the ASDP-BF533 Blackfin Processors



See processor's datasheet for more details

Power Consumption

- **Low Active Power**
  - **Low Power by process technology**
  - **Automatic power-down for unused peripheral sections**
- **Dynamic Performance Adaption**
  - **Modification of frequency and voltage by software**
    - Programmable PLL and Voltage Regulator
  - **5 Power modes**
    - Full-On, Active, Sleep, Deep-Sleep and Hibernate
- **See Power EE-Notes for more details**
  - **EE-298: Estimating Power for ADSP-BF538/BF539 Blackfin Processors**
  - **EE-297: Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors**
  - **EE-293: Estimating Power for ADSP-BF561 Blackfin Processors**
  - **EE-229: Estimating Power for ADSP-BF531/BF532/BF533 Blackfin Processors**
  - **EE-TBD: Estimating Power for ADSPBF542/BF544/BF547/BF548/BF549 Blackfin Processors**
  - **EE-TBD: Estimating Power for ADSP-BF523/BF525/BF527 Blackfin Processors**