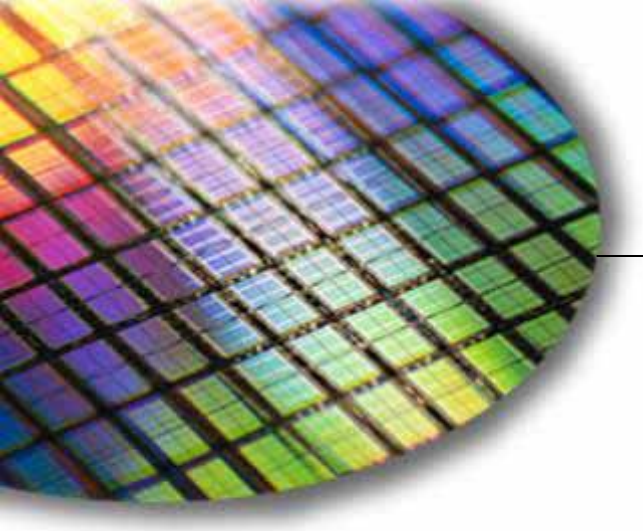


The World Leader in High Performance Signal Processing Solutions

Processors Q&A

March 2008
Rev 2.0

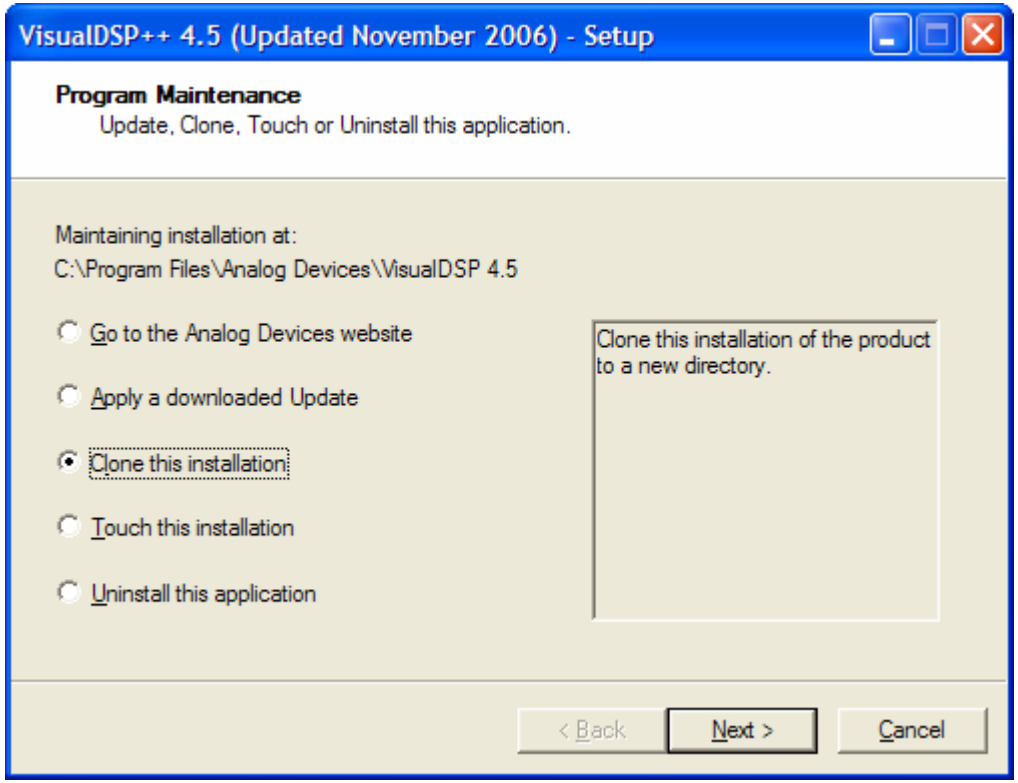
ANALOG DEVICES

Introduction

- **This presentation includes some common support requests that come in from customers and FAEs/DFAEs**
- **We will look at the best ways to approach the resolution of some of the most common questions**

Update of VDSP++

- **I have VDSP++ 5.0 update 1 installed. Like to install VDSP++5.0 update 2. Can I specify a directory so that Ver. 5.0 update 1 remains on the PC?**
  - **You do this via: Maintain Installation – Clone this installation**
  - **Then you have 2 versions on your PC. (1GB each version)**



Update from VDSP++ 4.5 to VDSP++ 5.0

- **I like to update to 5.0 but need to keep 4.5. Can I specify a specific directory?**
  - **No need to specify a directory**
  - **Version 5.0 goes into a new directory.**
  - **c:\Program Files\Analog Devices\VisualDSP 5.0**

Voltage Domains

- **Can I skip powering the voltage domains that I'm not using?**
  - **All power supply domains MUST be powered, even if associated function not used**
  - **For example, for a ADSP-BF52x design, you must power:**
    - VDDEXT, VDDUSB, VDDMEM, VDDOTP, VPPOTP
    - Special case: VDDRTC - Connect to VDDEXT if RTC not used

Power Supplies		
V_{DDEXT}	P	I/O Power Supply
V_{DDINT}	P	Internal Power Supply (regulated from 2.25 V to 3.6 V)
V_{DDRTC}	P	Real Time Clock Power Supply
V_{DDUSB}	P	3.3 V USB Phy Power Supply
V_{DDMEM}	P	MEM Power Supply
V_{DDOTP}	P	OTP Power Supply
V_{PPOTP}	P	OTP Programming Voltage

  - **See device datasheet for more details**
    - OPERATING CONDITIONS table

VDDOTP

- **In my ADSP-BF54x/BF52x design. Why do I need to provide 2.5V to VDDOTP if I'm not planning on using OTP memory?**
  - **You MUST provide 2.5 Volts for VDDOTP even if OTP is not being used**
  - **There are factory settings which are read from OTP at pre-boot time**
    - Factory trim values for the USB PHY controller, voltage regulator and SDRAM controller
    - Also, the factory settings prevent the boot ROM from accidentally accessing resources that are not present on a given product, which would result in unpredictable behavior and/or hardware errors

ADSP-BF52xC CODEC

- **What Codec device is used on the ADSP-BF52xC processors?**
  - **ADSP-BF527C1**
    - Initial ADSP-BF527C devices include a codec from Wolfson
      - Wolfson's Codec datasheet available upon request
    - X-Grade samples available now
    - Not going into production
  - **ADSP-BF527C2**
    - The codec that will eventually be included in all ADSP-BF52xC processors is an Analog Devices codec
      - A slightly modified version of the SSM2602 (sampling now)
      - The data sheet for that part can be found here:
        - http://www.analog.com/en/prod/0%2C2877%2CSSM2602%2C00.html
    - X-Grade samples: April 2008
    - Release to production: September 2008

ADSP-BF52x vs. ADSP-BF52xC Pin Compatibility

- **Can we do anything about pin compatibility between the ADSP-BF52x CODEC and non-CODEC versions?**
  - **Yes. There are signals which connect to the CODEC on the ADSP-BF52xC devices that cannot be left floating on the ADSP-BF52x devices without the CODEC**
  - **These signals may be tied to GND or VDDEXT**
  - **Therefore, boards designed for the ADSP-BF52xC may drop in a ADSP-BF52x without a problem**

Ball	BF52x	BF52xC
H22	GND	AGND
J22	VDDEXT or GND	AVDD
H17	VDDEXT or GND	VDDEXT
G17	GND	AGND
G16	VDDEXT or GND	AVDD

USB Peripheral Termination

- **How do I terminate the USB signals on my ADSP-BF54x/BF52x processor board when not using this peripheral?**
  - **When not using the USB peripheral, the following guide should be used:**
    - USB_DP = GND
    - USB_DM = GND
    - USB_XTALIN = GND
    - USB_XTALOUT = NC (No Connect)
    - USB_ID = GND
    - USB_VREF = NC
    - USB_RSET = NC
    - USB_VBUS = GND
  - **See the device datasheet**
    - Pin / Signal Descriptions table

USB HUB Support

- **Does the ADSP-BF54x/BF52x USB OTG interface support the use of a USB HUB?**
  - **In Peripheral mode**
    - Yes, it can connect to a standard USB host thru a hub…BUT
      - Hubs do not understand nor pass thru OTG functionality e.g. SRP, HNP
      - So if connected thru a hub, the processor is relegated to being a standard USB peripheral
  - **In Host mode**
    - No, Blackfin has a single-Point USB OTG controller
      - Cannot communicate with multiple devices thru a hub

USB Stack

- **I am looking for a USB stack for my ADSP-BF54x/BF52x based project. What are my options?**
  - **VisualDSP++ 5.0 Update 1 or later**
    - USB Peripheral Driver
    - USB Core API
    - Class drivers
      - Mass storage
      - Audio class driver is not yet available, planned for late summer
      - HID and other class drivers to be added in the future…
    - USB application examples:
      - Blackfin acting in Device (Peripheral) Mode:
        - Bulk Loopback Application
        - Bulk Redirect IO Application
        - Mass Storage Application
      - Blackfin acting in Host Mode:
        - VDK Shell Browser Application
  - **Jungo**
    - Full USB stack implementation ongoing…
    - More info available directly from Jungo @ www.jungo.com
  - **Micrium**
    - USB-Bulk stack
    - USB-MSD stack
    - More info available directly from Micrium @ www.micrium.com

USB Driver and Host OS Compatibility

- **Do the ADI USB drivers provided with VDSP++ 5.0 for ADSP-BF54x/BF52x support MAC operating systems, and in general, what is the support for other operating systems?**
  - **The USB mass storage driver support on Blackfin processors conforms to the mass storage device protocol**
  - **If an operating system such as MAC OS also conforms to this same protocol, then the USB driver should be compatible**
  - **The same information applies to the bulk storage drivers**

NAND Flash Booting

- **Do the ADSP-BF52x and ADSP-BF54x support NAND Flash boot mode?**
  - **ADSP-BF52x**
    - There is no native support for NAND Flash boot
    - It may be possible to take some portion of the NAND boot code customized for a specific NAND flash device and place it in OTP memory
    - The user could then boot from OTP and run the customized NAND boot code like a second-stage loader
    - Further investigation required...
  - **ADSP-BF54x**
    - Yes! There is native support for 8-bit and 16-bit NAND Flash boot
    - Example code available upon request

Mobile DDR

- **I like to interface the ADSP-BF548 to mobile DDR SDRAM. Is this supported?**
  - **Unfortunately, operation of Mobile DDR SDRAM memory (which typically operates at 1.8V) is not functional with the current silicon revision 0.1**
    - See anomaly 05000377
  - **We are investigating how and when mDDR can be enabled in revision 0.2**
  - **Updated information will be shared as it becomes available**

Host Boot Mode

- **In my ADSP-BF54x/BF52x application, I would like to boot from the host via the Host DMA Port. What is required?**
  - **Host DMA boot mode is a very special mode**
    - The Host DMA Port (HOSTDP) hasn‘t been architected to be a boot source
    - HOSTDP is not based on the boot kernel as other modes
    - All intelligence pushed out to the host
  - **Things to keep in mind:**
    - The host processor must be intelligent enough to parse the boot stream
    - The host processor must send an HIRQ (Host interrupt request) control command for init code blocks and for the final block
      - This information is contained in the boot block header
    - Transfers to the HOSTDP must always be multiples of FIFO depth
      - ADSP-BF54x - 64 bytes
      - ADSP-BF52x – 32 bytes

CAN Stack

- **Is there a CAN bus driver provided for Blackfin processors?**
  - **Currently, ADI has no plans to offer a CAN driver**
  - **The very basic CAN TX and CAN RX modules that ship in the EZ-KIT Examples directory within VisualDSP++ is all we can offer**
  - **For a fully functional CAN stack, refer to the 3rd party called Vector (http://www.vector-cantech.com/)**

SDK Based Project

- **I am trying to use the MJPEG encoder library from the SDK into my own project, but getting several compiler errors when building his project. How can I fix this?**
  - **Our recommendation is to either use the SDK example (including the LDF file) as a baseline for their application, and not the other way around**
  - **In your own project, you would need to review the SDK MJPEG LDF in order to duplicate the MJPEG memory placement requirements (as described in the Encoder Library Developer's Guide, Section 2.5, provided with the SDK) into their customized application**
    - This file shows the section names that must be added to the LDF file
  - **Additionally, the SDK libraries do not support the use of the Startup Code Wizard to generate the project and LDFs**
  - **Therefore, our recommendation is to start with the example provided in the SDK and adapt that to your purpose**

Compiler Efficiency

- **Is a comparison of your C Compiler efficiency/benchmarks and hand coded assembly available?**
  - **The Blackfin C/C++ compiler is an optimizing compiler and can be tuned for speed and code density**
  - **Since the compiler improves with each release, we do not do a study comparing the compiler-generated code to assembly programs**
  - **We recommend that all engineers use C/C++ as their programming language**
  - **There are ways to perform very low-level tasks through pragmas, intrinsic functions, and compiler switches**
  - **Inspecting the generated code is probably the best measure of compiler efficiency, and can be used to decide if hand-optimizing assembly functions is necessary**
    - VisualDSP++ Linear/Statistical profilers, cycle count macros, etc can assist with code benchmarking

MXVR and MOST

- **I have a question about the Media Transceiver (MXVR), which supports the MOST interface, on the Blackfin processors. Where can I obtain support for this peripheral?**
  - **The MXVR is a special peripheral available only on automotive products**
  - **Mocean Laboratories provides direct support of the MOST implementation**
    - adisupport@mocean-labs.com
  - **Direct link to ADI and can obtain any required information regarding the implementation on the Blackfin products required to address any customer inquiries**

Power Estimates (1 of 3)

- **Do you have any power estimates for the ADSP-BF548 processor?**
  - **ADSP-BF54x is currently available as X-Grade Rev 0.1 silicon**
  - **Characterization of this silicon is not complete and it is too early to have final characterization numbers for power**
  - **Characterization will be complete by release to production currently scheduled for May 30 2008 (Rev 0.1)**
  - **A power estimation application note for the ADSP-BF54x is planned**

Power Estimates (2 of 3)

- **Do you have any power estimates for the ADSP-BF527 processor?**
  - **ADSP-BF523/5/7 is currently available as X-Grade Rev 0.1 silicon**
  - **Characterization of this silicon is not complete and it is too early to have final characterization numbers for power**
  - **Characterization will be complete by release to production tentatively scheduled for September 2008 (Rev 0.2)**
  - **A power estimation application note for the ADSP-BF52x is planned**

Power Estimates (3 of 3)

- **Where can I get the latest power figures for my Blackfin design?**
  - **Refer to the EE-Notes available on the web (www.analog.com/ee-notes)**
    - EE-298: Estimating Power for ADSP-BF538/BF539 Blackfin Processors (Rev 1, 10/2006)
    - EE-297: Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors (Rev 2, 05/2007)
    - EE-293: Estimating Power for ADSP-BF561 Blackfin Processors (Rev 1, 10/2006)
    - EE-229: Estimating Power for ADSP-BF531/BF532/BF533 Blackfin Processors (Rev 3, 05/2007)
  - **For newest Blackfin processors, new EE-Notes will be made available when final device characterization is complete:**
    - EE-TBD: Estimating Power for ADSP-BF52x Blackfin Processors
    - EE-TBD: Estimating Power for ADSP-BF54x Blackfin Processors
    - In the mean time, some estimates are available
      - See Blackfin Applications Update slides...

ADSP-BF54x Hardware Reference Manual

- **When will the ADSP-BF54x HRM become available to the public?**
  - **We are planning on releasing the next update of the ADSP-BF54x HRM by the end of March**

__unknown_exception_occurred

- **My application jumps to __unknown_exception_occurred. What causes this and how do I resolve it?**
  - It is likely that an unhandled hardware event has occurred
  - On startup, all the entries in the Event Vector Table are set to point to __unknown_exception_occurred
  - It is most likely that a hardware exception has occurred
  - RETX register will give you the address of assembly line that the hardware exception occurred at
  - The EXCAUSE bits in SEQSTAT identify the cause of the exception

EZ-Extenders Support

- **What EZ-Extender boards can I use with my ADSP-BF548 EZ-KIT Lite? And with my ADSP-BF527 EZ-KIT Lite?**
  - **At the moment the only EZ-Extender boards that are supported by these kits are the ADZS-BFFPGA-EZEXT and ADZS-BFAV-EZEXT**

Blackfin L1 Boot ROM

- **Can I custom mask the L1 Boot ROM on my ADSP-BF54x/BF52x processor?**
  - **L1 Boot ROM is not user configurable**
  - **Area reserved for boot ROM code and security code**
  - **Should we decide to make available custom ROM for ADSP-BF54x/BF52x devices in the future, similar requirements to those offered for other ADI products would apply (guideline data):**
    - $50k NRE
    - >50k Yr Minimum Quantity
    - 3 Yr Minimum Commitment

SHARC ROM (1 of 3)

- **I am interested in using some of the audio algorithms available in the ADSP-21366 internal ROM. What is required?**
  - **SHARC Processors with Audio Algorithms in ROM: ADSP-21266, ADSP-21365, ADSP-21366, and ADSP-21367**
  - **ADSP-21362 only contains a DTCP engine (DTLA license required) - automotive only**
  - **ADSP-21371 only contains coefficients for some of the below audio algorithms**
  - **Available algorithms (factory mask-programmed)**
    - PCM
    - Dolby Digital*, Dolby Digital EX2*, Dolby Pro Logic IIx*
    - DTS 5.1*, DTS ES*, DTS Neo:6*, DTS 96/24*
    - SRS Focus*
    - MPEG2 AAC LC
    - MP3
    - Graphic Equalizer, Balance/Fader, Bass Management, Delay Management
  - **Requirements:**
    - License agreement required from IP* holders prior to receipt of silicon samples
    - No minimum quantity
    - No NRE costs

SHARC ROM (2 of 3)

- **I am interested in programming the ADSP-21364 internal ROM with his own code. Is this possible? What is required?**
  - **Supported SHARC Devices for custom masked ROM are:**
    - ADSP-21363, ADSP-21364, ADSP-21369 and ADSP-21371
  - **Requirements:**
    - Minimum quantity (general guideline): 50k pieces
    - One-time NRE costs (general guideline): $75K
    - The Customer is responsible for the software in the ROM
    - ADI will only put their code in the ROM but are not responsible for the functionality

SHARC ROM (3 of 3)

- **Is it possible to boot the ADSP-21363 from internal ROM?**
  - **Internal boot mode is not a generic boot mode**
  - **However, this boot mode is supported for custom ROM devices**
    - ADSP-21363, ADSP-21364, ADSP-21369 and ADSP-21371
  - **Otherwise, by default, the ROM doesn't include any useful boot code and your boot choices are:**
    - SPI Slave Boot
    - SPI Master Boot
    - Parallel Port Boot via EPROM/Flash

SHARC Processors Pin Compatibility (1 of 2)

- **What devices is my ADSP-21369 SHARC processor pin compatible with?**
  - **ADSP-21368 and ADSP-21369 SBGA packages are pin compatible**
  - **ADSP-21371/5 and ADSP-21369 EP_LQFP packages are pin compatible**

SHARC Processors Pin Compatibility (2 of 2)

- **If using SDRAM, and it is for the ADSP-21371 processor you need to specify the SDRAM External Data Path Width (SDCTL Bit 16: X16DE - ADSP-21371 only) to be of the same width as for the ADSP-21375 SDRAM interface**
- **By default, this bit is set to 0 (1=16 bits, 0=32 bits), so you would need to change it to 1, to enable a 16-bit SDRAM interface.**
  The ADSP-21371 and ADSP-21375 processors are pin compatible
- **You can use the ADSP-21371 (bigger family member) to get started and then move to the ADSP-21375 (smaller family member) without any problems**

Product Status and Samples Availability Scenario

- **Can you tell me when is the ADSP-BF527 going to be released to production? Speed grade? Package type? Temperature grade?**
  - **For product status update and/or samples availability, whether it is for ENG, X-Grade, or production silicon:**
    - NOTE: For pre-production silicon, an ENG and/or X-Grade agreement needs to be in place before we can ship silicons

Summary

- **Any other questions?**

Thanks

ANALOG DEVICES